a sense amplifier for sensing the position of the measurement mass within the sensor.

31 ~~4~~. The apparatus of claim 28 ~~1~~, wherein the controller further comprises:

a loop filter for providing control to the sensor apparatus, to the loop filter including:

one or more integrators for providing a signal for controlling the sensor system;

one or more derivative controllers for providing a signal for controlling the sensor system;

one or more proportional controllers for providing a signal for controlling the sensor system; and

a summer for combining the signals from the integrators, the derivative controllers, and the proportional controllers.

32 ~~5~~. The apparatus of claim 26 ~~1~~ further comprising:

a multiphase clock generator for providing clock signals for controlling the operation of the apparatus, the clock generator including:

a digital signal generator; and

a data-independent clock resynchronization circuit coupled to the digital signal generator for resampling clock signals.

33 ~~6~~. The apparatus of claim 28 ~~1~~ further comprising:

a sensor simulator for simulating the operation of a sensor, the simulator including;

a filter adapted to receive one or more input signals and generate an output signal representative of the operating state of the sensor; and

an input signal selector operably coupled to the filter adapted to controllably select the input signals as a function of the simulated operating state of the sensor.

34 ~~7~~. The apparatus of claim 28 ~~1~~ further comprising:

a device for testing the operation of the controller, the device comprising;

a sensor simulator for simulating the operation of a sensor; and

a second controller coupled to the simulator.

35 ~~8~~. The apparatus of claim 28 ~~1~~, wherein the controller further comprises:

a feedback control system for providing control to the apparatus, the feedback control system comprising:

a startup sequencer for selecting the mode of operation of the feedback control system; and

a loop filter coupled to the startup sequencer.

36 ~~6~~. The apparatus of claim 35 ~~5~~, wherein the clock resynchronization circuit comprises:

a plurality of inverters;

a plurality of NOR gates coupled to the inverters;

a plurality of NAND gates coupled to the inverters;

a plurality of XNOR gates coupled to the NAND gates and the inverters;

a plurality of asynchronous set double-edge flip-flops coupled to the NOR gates; and

a plurality of asynchronous reset double-edge flip-flops coupled to the NOR gates.

37 ~~10~~. A method of controlling the operation of a sensor assembly, comprising:

using a controller to apply electrostatic forces to a sensor to create one or more sensor operating states; and

sequentially arranging the operating states into which the sensor is placed to create a plurality of operating modes for the sensor assembly.

38 ~~11~~. The method of claim 37 ~~10~~ further comprising:

determining an operating mode of the sensor assembly;

adjusting a mode of operation of a loop filter in the sensor assembly;

providing feedback loop compensation to the sensor assembly during a start-up mode of operation for the sensor assembly; and

providing noise shaping to the sensor assembly during a sigma-delta mode of operation for the sensor assembly.

39 ~~12~~. The method of claim 37 ~~10~~, wherein the sensor assembly includes a loop filter, one or more integrators, a proportional controller, the method further comprising:

placing a loop filter including one or more integrators, a proportional controller, and a derivative controller in a reduced-order operating mode;

sending a signal to the loop filter to control the operating mode of the loop filter; and

holding the integrators within the loop filter in a reset mode to place the loop filter in the reduced-order operating mode.

40 ~~13~~. The method of claim 39 ~~12~~ further comprising:

taking the integrators out of the reset mode to place the loop filter in a normal operating mode when the sensor system is operating in a sigma-delta operating mode.

41 ~~14~~. The method of claim 39 ~~12~~, wherein the operating mode of the loop filter further comprises:

sending a signal to the loop filter indicating an operating mode of the sensor assembly;

operating the loop filter in a reduced-order mode while the sensor assembly is operating in a start-up mode;

operating the loop filter in the reduced-order mode for a predetermined period of time after the sensor assembly transitions from the start-up operating mode to a sigma-delta operating mode; and

operating the loop filter in a normal mode during the sigma-delta operating mode after the predetermined period of time during which the loop filter operates in reduced-order mode.

42 ~~15~~. The method of claim 41 ~~14~~, wherein the operating mode of the loop filter further comprises:

operating the loop filter in a reduced-order mode while the sensor assembly is operating in the sigma-delta operating mode.

43 ~~16~~. The method of claim 37 ~~10~~ further comprising:

generating a clock signal for the sensor assembly, the generating including:

generating a first clock signal; and

resampling the first clock signal to generate a second clock signal to restore signal integrity and providing a timing relationship.

44 ~~17~~. The method of claim 37 ~~10~~ further comprising:

resampling an input signal to the sensor assembly, the resampling including:

resampling the input signal in a first level-sensitive latch, including one or more transmission gates, one or more NOR gates, and one or more inverters, on one edge of a clock input signal; and

resampling the input signal in a second level-sensitive latch, including one or more transmission gates, one or more NOR gates, and one or more inverters, acting in parallel with the first level-sensitive latch, on another edge of the clock input signal.

45 ~~18~~. The method of claim 37 ~~10~~ further comprising:

resampling an input signal to the sensor assembly, the resampling including:

resampling the input signal in a first level-sensitive latch, including one or more transmission gates, one or more NAND gates, and one or more inverters, on one edge of a clock input signal; and

resampling the input signal in a second level-sensitive latch, including one or more transmission gates, one or more NAND gates, and one or more inverters, acting in parallel with the first level-sensitive latch, on another edge of the clock input signal.

46 ~~19~~. The method of claim 37 ~~10~~, wherein the controller includes an analog control circuit, the method further comprising:

operating the analog control circuit by generating a first clock signal;

resampling the first clock signal to generate a second clock signal to restore signal

integrity and provide a proper timing relationship; and

driving the analog control circuit using the second clock signal.

47 ~~20~~. The method of claim ~~10~~ 37 further comprising testing the controller, wherein the test comprises:

connecting a sensor simulator to the controller;

supplying an input signal of a known value to the sensor simulator;

converting the input data to the sensor simulator into an output stream from the sensor simulator;

sending the output stream from the sensor simulator to the controller;

processing the output stream from the sensor simulator within the controller to create an output stream from the controller; and

analyzing the output from the controller to determine the accuracy of the controller.

48 ~~21~~. The method of claim ~~10~~ 37 further comprising:

offsetting the effects of external acceleration forces on the sensor assembly independent of sensor assembly orientation by applying electrostatic forces to a sensor element to offset the effects of the acceleration force.

Respectfully submitted,

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